REMARKS

I. Introduction

In response to the Office Action dated June 30, 2006, Applicants have canceled claims 2 – 7, and have amended claims 1, 8, 11, and 12 to more particularly point out and distinctly claim the subject matter of the invention. No new matter has been added.

In view of the foregoing amendments and the following remarks, Applicants respectfully submit that all pending claims are in condition for allowance.

II. Claim Rejections Under 35 U.S.C. § 103

Claims 1 – 3 and 5 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,400,625 to Arimoto in view of U.S. Patent No. 6,552,936 to Shiga. Claims 4 and 6 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Arimoto, Shiga, and U.S. Patent Application Publication No. 2002/0141280. Claims 7, 8, 11, and 12 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Arimoto, Shiga, and U.S. Patent No. 6,157,992 to Sawada. Claim 9 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Arimoto, Shiga, and U.S. Patent no. 6,002,627 to Chevalier. Claim 10 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Arimoto, Shiga, and U.S. Patent No. 6,437,308 to Koh. Applicants traverse these rejections for at least the following reasons.

Claim 1 recites, among other things, a storage device comprising a timing signal output circuit for outputting a timing signal indicative of a timing that is shifted by a first predetermined time period which is determined according to a frequency of a clock signal which allows reading of data and a read data control circuit for performing control on the timing signal for outputting the data read from the memory to the microcomputer, wherein the read data control circuit

performs control such that the microcomputer takes in the output from the mask circuit only when the clock signal has a frequency between an upper limit and a lower limit determined according to a first and second timing period. At least these features are not disclosed or suggested by the cited references, alone or in combination with each other.

The Examiner asserts that Arimoto discloses a timing signal output circuit for outputting a timing signal indicative of a timing that is shifted by a predetermined time period, which is determined according to a frequency of the clock signal. It appears that the Examiner has misunderstood the term frequency recited in claim 1. Accordingly, Applicants have amended claim 1 to more particularly recite that frequency refers to the frequency which allows reading of data. Clearly, Arimoto fails to disclose a timing signal output circuit which outputs a timing signal indicative of a timing shifted by a time period determined according to the frequency of a clock signal which allows the reading of data.

The Examiner refers to a data shifter which shifts test output data transmitted from a read data selection circuit for a period corresponding to a generated timing control signal. However, the period corresponding to a timing control signal Q generated by a mode register 2 has nothing to do with the frequency of the clock signal which allows reading of data, as recited in claim 1.

Shiga does not overcome this deficiency. Furthermore, Shiga fails to disclose a read data control circuit controlling the microcomputer based on an upper limit and a lower limit determined according to a first and second timing period. Shiga appears to disclose that an upper limit of the frequency is determined by a value which can be continuously output without delay in a pipeline operation. The Examiner asserts that Shiga discloses that during reading of a slow period, when the timing is prepared by the external clock, undesireable problems such as a

wastefully long-time biased cell are generated in reliability. However, Shiga does not disclose or even suggest that a frequency which allows reading of data has a lower limit.

Claim 11 recites, among other things, a storage device comprising a mask circuit for outputting data read from the memory to the microcomputer for a predetermined time period less than each one read cycle and a timing control circuit for performing control such that the predetermined time period less than each one read cycle during which the mask circuit outputs the data read from the memory and the timing for taking the data output from the mask circuit into the microcomputer correspond to each other and are variable. The Examiner admits that Arimoto and Shiga fail to disclose this feature, and relies on Sawada to overcome this deficiency.

Sawada appears to be directed to a memory device having a control portion which controls data output. The Examiner refers to a mask enable circuit disclosed by Sawada which delays an internal mask instructing signal for a predetermined period of time. However, the process of delaying the internal mask signal is irrelevant to the frequency of the clock signal which allows reading of data. Furthermore, Sawada is silent regarding a microcomputer taking in data output from the mask circuit at a predetermined timing.

Accordingly, as each and every limitation must be disclosed or suggested by the prior art references in order to establish a *prima facie* case of obviousness (MPEP § 2143.03), and the combination of the cited references fails to do so, it is respectfully submitted that independent claims 1 and 11 are patentable over the cited references taken alone or in combination with one another.

Claims 8 – 10 and 12 depend from one of independent claims 1 and 11. Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the

dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,* 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as independent claims 1 and 11 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

III. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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